IN THE CLAIMS

Please amend claims 79, 80 and 86 as set forth below.

Claims 1-78 (cancelled)

79.(Currently amended) A lateral MOSFET for an integrated circuit comprising:

a substrate;

a relativcly thin layer of dielectric formed on a surface of the substrate;

a first region of relatively thick material formed on the surface of the substrate adjacent the relatively thin dielectric material having a predefined lateral length, wherein the first region can mask dopants from penetrating the surface of the substrate;

a first top gate of a first conductivity typed formed in the substrate adjacent the surface of the substrate; and

a drain contact region of a second conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate~~; and~~

~~a first top gate of a first conductivity typed formed in the substrate adjacent the surface of the substrate~~, the distance between the drain contact region and the first top gate is defined by the lateral length of the first region.

80. (Currently amended) The lateral MOSFET for an integrated circuit of claim 79, further comprising:

a gate material region formed on the relatively thin dielectric material, wherein the gate material is used as a mask to form an ~~second~~ edge of the first top gate.

81. (Original) The lateral MOSFET of claim 79, further comprising:

a body region of the first conductivity type formed in the substrate adjacent the surface of the substrate;

a source of the second conductivity type with high dopant density formed in the body region; and

a body contact of the first conductivity type with high dopant density formed in the body region adjacent the source.

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82. (Original) The lateral MOSFET of claim 79, wherein the drain contact region is formed deeper from the surface of the substrate than the first top gate, further wherein the drain contact has a higher dopant concentration at every depth from the surface of the substrate than the first top gate.

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83. (Original) The lateral MOSFET of claim 79, further comprising:

a main drift region of the second conductivity type formed around the first top gate and extending beyond the drain contact.

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84. (Original) The lateral MOSFET of claim 83, wherein the main drift region further comprises:

a first drift region formed by implanting dopants of the second conductivity type into the substrate using a first edge of the first region as a mask; and

a second drift region formed by implanting dopants of the second conductivity type into the substrate using a second edge of the first region as a mask, wherein the dopants of the first and second drift regions are diffused under the first region to form the main drift region.

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85. (Original) The lateral MOSFET of claim 83, further comprising:

a well of the second conductivity type formed under first region to reduce resistance in the main drift region.

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86. (Currently amended) The lateral MOSFET of claim 79, further comprising:

a first drift region of the second conductivity type in the substrate extending from the a first edge of the first region to beyond the first top gate; and

a second drift region of the second conductivity type extending from the a second edge of the first region beyond the drain contact.

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~~87~~. (Original) The lateral MOSFET of claim ~~86~~, further comprising:

a first conductivity well of the second conductivity type formed under first region in the substrate to reduce resistance in the first and second drift regions.

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~~88~~. (Original) The lateral MOSFET of claim ~~79~~, further comprising:

a second region of relatively thick material formed on the surface of the substrate a predetermined distance from the first region, wherein the lateral length of the drain contact region is defined by the distance between the first and second regions.

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~~89~~. (Original) The lateral MOSFET of claim ~~88~~, further comprising:

a second top gate of the first conductivity type formed in the substrate adjacent the surface of the substrate, wherein the distance between the drain contact region and the second top gate is defined by the lateral length of the second region.

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~~90~~. (Original) The lateral MOSFET of claim ~~88~~, wherein the first region of relatively thick material is connected to the second region of relatively thick material, the first and second regions of relatively thick material having a central opening, the drain contact region is positioned adjacent the central opening.

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~~91~~. (Original) The lateral MOSFET of claim ~~90~~, wherein the first top gate extends around an outer perimeter of the first and second regions of relatively thick material.

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~~92~~. (Original) The lateral MOSFET of claim ~~89~~, wherein the drain contact region is formed deeper from the surface of the substrate than the first and second top gates and has a higher dopant concentration at every depth than first and second top gates.

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~~93~~. (Original) The lateral MOSFET of claim ~~89~~, wherein the first and second relatively thick materials are made from a dielectric material.

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94. (Original) The lateral MOSFET of claim 89, wherein the first and second relatively thick materials are made from a gate material.

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95. (Original) The lateral MOSFET of claim 94, wherein the first and second regions are left floating.

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96. (Original) The lateral MOSFET of claim 94, wherein the first and second regions are coupled to the drain contact region.

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97. (Original) A lateral MOSFET for an integrated circuit comprising:

a substrate;

a relatively thick dielectric region formed on a surface of the substrate, the relatively thick dielectric region having a predetermined lateral length;

a relatively thin dielectric region formed on the surface of the substrate;

a gate electrode deposited on the relatively thin dielectric region;

a first top gate region of a first conductivity type formed in the substrate adjacent the surface of the substrate and between the gate electrode and the relatively thick dielectric region;

a drain region of a second conductivity type having a high doping density formed in the substrate adjacent the surface of the substrate and adjacent the relatively thick dielectric region, wherein the lateral width of the relatively thick dielectric region defines the lateral distance between the first top gate region and the drain region; and

a source region of the second conductivity type having a high doping density formed in the substrate adjacent the surface of the substrate, wherein the gate electrode is laterally positioned between the source region and the first top gate.

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98. (Original) The lateral MOSFET for an integrated circuit of claim 97, further comprising:

a body region of the first conductivity type formed in the substrate adjacent the surface of the substrate and the source region; and

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a body contact of the first conductivity type having a high dopant density formed in the body region adjacent the surface of the substrate and a portion of the source region.

21 99. (Original)The high power lateral MOSFET for an integrated circuit of claim 19 further comprising:

a drift region of the second conductivity type formed in the substrate adjacent a surface of the substrate and the first top gate and drain region.

22 100. (Original) The lateral MOSFET for an integrated circuit of claim 19, wherein the drain region is formed to extend deeper from the surface of the substrate than the first top gate, further wherein the drain region is formed with a higher doping density at every depth than the first top gate.

23 101. (Original) The lateral MOSFET for an integrated circuit of claim 19, wherein the source region is formed to extend deeper form the surface of the substrate than the first top gate, further wherein the source region is formed with a higher dopant density at every depth than the first top gate.

24 102. (Original) The lateral MOSFET for an integrated circuit of claim 19, further comprising:

a first drift region of the second conductivity type formed in the substrate adjacent the relatively thick dielectric layer and the drain region; and

a second drift region of the second conductivity type formed in the substrate adjacent the first top gate and the relatively thick dielectric layer, wherein the first and second drift regions overlap under the relatively thick dielectric layer.

25 103. (Original) The lateral MOSFET for an integrated circuit of claim 24, further comprising:

a well of the second conductivity type formed in the substrate adjacent the overlapping area of the first and second drift regions to reduce resistance in the first and second drift regions.

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104. (Original) The lateral MOSFET for an integrated circuit of claim 102, further comprising:

a second top gate of the first conductivity type formed in the substrate adjacent the surface of the substrate and a predetermined distance from the drain region to form a single multistripe device in the integrated circuit, wherein the well extends from a portion of the first top gate to a portion of the second top gate.

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105. (Original) The lateral MOSFET for an integrated circuit of claim 97, wherein the relatively thick dielectric region has a central opening, the drain region is laterally positioned in the central opening.

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106. (Original) The lateral MOSFET for an integrated circuit of claim 105, wherein the first top gate is laterally positioned around an outside perimeter of the relatively thick dielectric region.

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107. (Original) A solid state relay integrated circuit comprising:

a photo diode stack to drive a voltage having a first output and a second output;

a first high voltage MOSFET having a gate, source and drain, the gate of the first high voltage MOSFET is coupled to the first output of the photo diode stack, the source of the first high voltage MOSFET is coupled to the second output;

a second high voltage MOSFET having a gate, source and drain, the gate of the second high voltage MOSFET is coupled to the first output of the photo diode stack, the source of the second high voltage MOSFET is coupled to the second output of the photo diode stack; and

wherein the first and second high voltage MOSFETs comprise,

a substrate,

a relatively thin layer of dielectric formed on a surface of the substrate,

a first region of relatively thick material formed on the surface of the substrate adjacent the relatively thin dielectric material having a predefined lateral length, wherein the first region can mask dopants from penetrating the surface of the substrate,

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a drain contact region of a second conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate, wherein the first region is used as a mask to form a first edge of the drain contact, and

a first top gate of the first conductivity typed formed in the substrate adjacent the surface of the substrate, wherein the first region is used as a mask to form a first edge of the first top gate, further wherein the distance between the drain contact region and the first top gate is defined by the lateral length of the first region.

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108. (Original) The solid state relay circuit of claim 107, wherein each of the drain contact regions of the first and second MOSFETs is formed to extend deeper from the surface of the substrate than the associated top gate, further wherein each drain region is formed with a higher doping density at every depth than an associated top gate.

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109. (Original) The solid state relay circuit of claim 107, further comprising:

a turn off and gate protection circuit coupled in parallel with photo diode stack to discharge any gate source capacitance when the photo diode stack is not driving voltage to the first and second high voltage MOSFETs.

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110. (Original) The solid state relay of claim 107, further comprising:

a first switch terminal coupled to the drain of the first high voltage MOSFET; and

a second switch terminal coupled to the drain of the second high voltage MOSFET.

Claims 111 -126 (cancelled)